APPLIED SCIENCES AND ENGINEERING

Stretchable complementary integrated electronics based on elastic dual-type transistors

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Complementary integrated circuits in an elastic format are essential for systems toward emerging applications in wearable health monitors, soft robotics, and implantable medical devices. However, their development is very nascent, largely owing to the imbalance of p- and n-type elastic transistors. Here, we report fully stretchable complementary integrated electronics combining elastic n-type transistors based on metallic carbon nanotube (CNT)–oped poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} with p-type transistors using semiconducting CNT networks. The layered elastomer-semiconductor-elastomer architecture provides both type transistors with stable, well-matched electrical characteristics up to 50% strain. Using these components, we demonstrate stretchable digital logic gates—including inverters, NAND, and NOR—which retain function under large strain. As a system-level demonstration, a complementary inverter active matrix integrated with a single-electrode triboelectric nanogenerator array realizes a stretchable tactile sensing skin. The stretchable complementary integrated electronics demonstrated here hold promise in many fields, particularly these require seamless integration with dynamic living systems.

INTRODUCTION

Complementary integrated electronics are essential for achieving logic functionality, low power consumption, and scalability in electronic systems (*1*–*6*). Realizing these capabilities in fully stretchable elastic format is critical for emerging applications such as wearable health monitors, soft robotics, and implantable medical devices, which demand electronic components that can mechanically deform without performance loss (*7*–*11*). Although stretchable complementary metal-oxide semiconductor circuits based on silicon nanomembranes and architecture engineering strategies have been reported, such approaches relied on rigid materials and structural accommodation of strain (*12*–*16*). Hence, they lack true material-level elasticity and are not suitable for intimate, conformal integration with soft biological tissues or dynamically deformable surfaces (*17*, *18*). Despite progress in developing rubbery stretchable transistors (*8*, *19*, *20*), fully stretchable complementary integrated electronics and its logic circuits requiring both p-type and n-type transistors remain nascent. Most efforts to date have focused on p-type stretchable semiconductors (*8*, *10*, *21*–*23*), while stretchable high-performance n-type counterparts remain underdeveloped. Specifically, n-type materials tend to have lower electron mobility and higher sensitivity to strain and environmental degradation compared to their p-type counterparts (*24*–*28*). As a result, achieving n-type rubbery semiconductors that match the mechanical and electronic performance of p-type systems has been difficult, impeding the realization of balanced, stretchable complementary system. The asymmetry presents a fundamental bottleneck in achieving reliable stretchable complementary integrated electronics.

Here, we report the development of stretchable complementary integrated electronics and logic circuits by designing scalable, stretchable n-type and p-type transistors that maintain stable electrical performance under mechanical strain. For the stretchable n-type transistors, we used metallic carbon nanotubes (m-CNTs) to dope poly{[*N*,*N*′-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,5′-(2,2′-bithiophene)} [P(NDI2OD-T2), or N2200], while the p-type transistors were fabricated using diluted semiconducting CNTs (s-CNTs) to achieve comparable electrical properties. Owing to the unique layered architecture of elastomer-semiconductor-elastomer, both n-type and p-type transistors demonstrate stable performance under mechanical strains of up to 50%, overcoming the trade-offs between mechanical robustness and electronic performance. We found that the stacked device structure of the stretchable n-type transistors and the s-CNT network in the stretchable p-type transistors provide the mechanical robustness necessary to maintain high carrier mobility and stable operation under mechanical deformation. In addition, we developed stretchable complementary digital circuits, including inverter (NOT), NAND, and NOR gates, which retained stable electrical characteristics under 30% strain. To demonstrate the applicability of these systems, we created a stretchable tactile sensing skin that integrated a complementary inverter active matrix with a single-electrode triboelectric nanogenerator (s-TENG) array. This platform for stretchable integrated electronics presents a promising path toward highly integrated, soft devices for many applications ranging from biointegration to robotic interfaces and others.

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RESULTS

Thin film transistor based on m-CNT–doped N2200 and s-CNTs

Figure 1A presents the exploded schematic view of the thin film transistor and molecular structure of the semiconductors used for channels. The device comprises a silver nanowire (AgNW)/polydimethylsiloxane (PDMS) elastomeric conductor, m-CNT–doped N2200 or s-CNT, polyurethane (PU), and eutectic gallium-indium (EGaIn) as source and drain electrode, semiconductor, gate dielectric, and gate electrode, respectively. The fabrication process involves sequential deposition and patterning of each component. Initially, the source and drain electrodes were prepared via our previously reported protocol (*8*, *17*, *29*). Subsequently, the semiconductor layer was deposited between the source and drain electrodes, and a 22-μm-thick transparent PU dielectric layer was spin coated and patterned over the channel region (fig. S1). Under 50% mechanical strain, the PU dielectric exhibited excellent stretchability (fig. S2). Capacitance measurements under different strain levels and frequencies revealed an initial capacitance of 14.77 pF/mm^2 at 1 kHz, which showed a slight increase with elongation, attributable to a reduction in dielectric thickness (fig. S3) (*21*, *30*). Last, the gate electrode was patterned using EGaIn via a shadow mask technique.

Figure 1B presents an optical image of the thin film transistors, with each material labeled according to the schematic in Fig. 1A. The stretchable n-type transistors were fabricated using m-CNT–doped N2200, while the stretchable p-type transistors used s-CNTs. Figure 1B also illustrates the carrier mobility enhancement mechanism in the n-channel. Incorporating m-CNTs into N2200 improves charge carrier transport due to the high electrical conductivity of m-CNTs. The m-CNTs bridge the crystallites formed by N2200, providing a low-resistance pathway for electron transport,

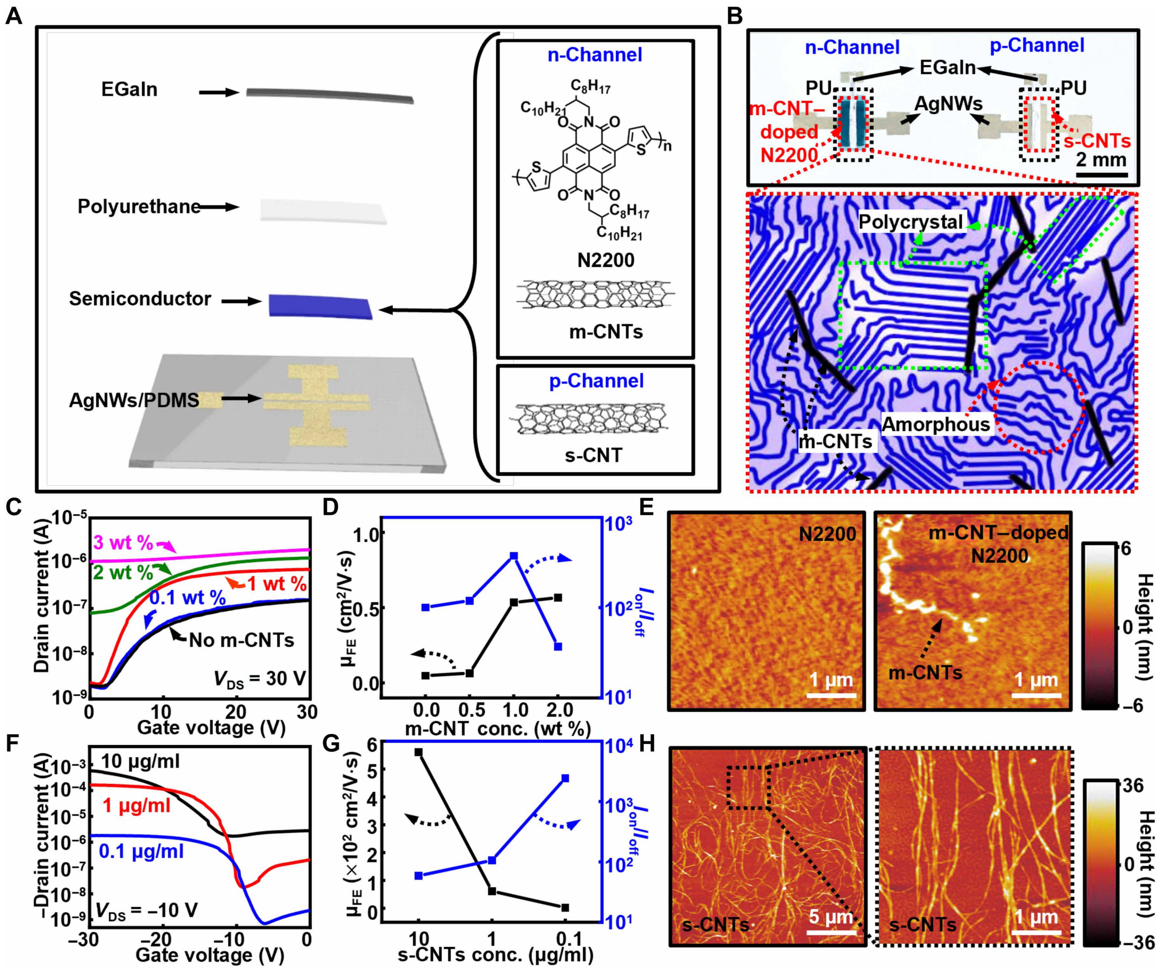

Fig. 1. Materials, characterization, and fabrication. (**A**) Exploded schematic view of the stretchable transistor layered structure (left) and molecular structure of the semiconductors used in the channel (right). m-CNT–doped N2200 and s-CNTs were used for n-channel and p-channel, respectively. (**B**) Optical image of fabricated stretchable transistors and schematic illustration of charge carrier transport in the n-channel. The top left shows the stretchable n-type transistor fabricated from m-CNT–doped N2200, and the top right shows the stretchable p-type transistor fabricated from s-CNTs. (**C**) Transfer characteristics of stretchable n-type transistors fabricated from N2200 doped with different concentrations of m-CNTs. (**D**) Field-effect mobility (μ_{FE}) and on/off current (I_{on}/I_{off}) of stretchable n-type transistors fabricated from N2200 doped with different concentrations of m-CNTs. (**E**) Atomic force microscopy (AFM) images of pristine N2200 film (left) and m-CNT–doped N2200 film (right). (**F**) Transfer characteristics of stretchable p-type transistors fabricated from different s-CNT concentrations. (**G**) μ_{FE} and I_{on}/I_{off} of stretchable p-type transistors fabricated from different s-CNT concentrations. (**H**) AFM images of s-CNTs.

which leads to an increase in effective mobility (*29*, *31*). However, as the concentration of m-CNTs increases, the formation of a percolated conductive network leads to excessive channel current even when the device is off, adversely affecting its performance.

On the basis of this understanding, we optimized the performance of the stretchable n-type transistors by adjusting the concentration of m-CNTs doped in N2200. Figure 1C shows the transfer characteristics of these devices obtained by sweeping the gate voltage from 0 to 30 V under a constant drain-source voltage (V_{DS}) of 30 V. The output characteristics are provided in fig. S4. As shown in Fig. 1D, increasing the m-CNT concentration to 1 wt % resulted in a substantial improvement in effective field-effect mobility (μ_{FE}), rising from 0.048 to 0.534 cm^2/V·s while maintaining the current on/off ratio (I_{on}/I_{off}). However, when the m-CNT concentration exceeded ~3 wt %, the gate-dependent field-effect behavior became significantly suppressed, and the output characteristics became linear, consistent with the formation of continuous conductive pathways and the transition toward metallic-like transport. Atomic force microscopy (AFM) images revealed that the pristine N2200 film formed a continuous nanofibril structure with a root mean square (RMS) roughness of 0.9 nm (Fig. 1E) (*32*). The RMS increased slightly (~1.2 nm) after doping with m-CNTs, due to nanotube aggregation, yet the film retained its nanofibril structures, indicating that m-CNTs bridge the N2200 crystallites without compromising the morphology. The homogeneous distribution of m-CNTs in the N2200 film supports the proposed charge carrier enhancement mechanism in the n-channel (fig. S5).

Achieving comparable performance in p-type transistors relative to their n-type counterparts is essential for constructing complementary circuits. To address this, we fabricated stretchable p-type transistors with varying s-CNT concentrations. Figure 1F shows that reducing the s-CNT concentration from 10 to 0.1 μg/ml lowered the on current (I_{on}) from 5.7×10^{-4} to 1.8×10^{-6} A, comparable to the current level of the stretchable n-type transistors. Figure 1G summarizes the μ_{FE} and I_{on}/I_{off} of the stretchable p-type transistors across different s-CNT concentrations. The reduction in I_{on} and μ_{FE}, along with the increase in I_{on}/I_{off}, was primarily attributed to the density of s-CNTs in the channel (*33*, *34*). The output characteristics of the stretchable p-type transistor are shown in the fig. S6. Surface morphology analysis revealed a network structure, with individual s-CNTs having a width of 40 to 50 nm (Fig. 1H). The optimization of both stretchable n-type and p-type transistors, achieved by tuning charge carrier mobility and controlling current, has resulted in balanced performances, a critical prerequisite for developing complementary circuits.

Stretchable n-type and p-type transistors with their arrays

The mechanical compliance of the stretchable transistors was evaluated under mechanical stretching both perpendicular and parallel to the channel length directions. Figure 2 (A and B) shows the stretchable n-type transistors (top: m-CNT–doped N2200) and p-type transistors (bottom: s-CNTs) under 0, 10, 30, and 50% strain in both directions. The representative transfer curves of both stretchable transistors under 0, 10, 30, 50, and 0% released (Re) strain are presented in Fig. 2 (C and F) (perpendicular) and Fig. 2 (D and G) (along). The μ_{FE} was extracted from the saturation region, accounting for the deformed channel geometries and the increased dielectric capacitance. Figure 2 (E and H) summarizes the changes in μ_{FE} and threshold voltage (V_{th}) changes under strains for both stretchable transistors. The mobility decreased more rapidly in the perpendicular direction and partially recovered upon release to 0% strain. Tables S1 and S2 provide detailed μ_{FE} and V_{th} data, confirming the stable and reliable operation of both stretchable transistors under high mechanical strain. We next subjected both n-type and p-type transistors to 1000 cycles of 50% uniaxial stretch-release. Figure S7 shows a gradual shift in V_{th} and decrease in mobility. Although mobility decreases under 50% strain, the devices maintained well-defined transfer characteristics and $I_{on}/I_{off} > 10^2$ throughout the cycling. These results highlight that “mechanical stability” in our system refers to the preservation of electrical switching functionality under strain, rather than constant mobility.

Forward and reverse gate sweeps under 0 and 50% strain revealed that the change in hysteresis window increased from 0.32 to 4.11 V for the n-type and p-type transistors, respectively (fig. S8). This strain-enhanced hysteresis likely arises from increased trap density or interfacial modifications, which collectively contribute to the mobility degradation observed under mechanical deformation. However, this hysteresis does not indicate instability during repeated switching. When the same gate sweep was applied over 10 consecutive cycles, both transistors exhibited only minor changes in V_{th} and mobility (fig. S9), confirming stable behavior without progressive degradation. Under prolonged gate bias (±30 V), both transistors displayed gradual electrical shifts and reduced on current (fig. S10) yet consistently retained gate modulation and reliable switching performance throughout. In addition, environmental stability was assessed by exposing both device types to ambient air for 4 days. As shown in fig. S11, only slight shifts in threshold voltage and moderate mobility reductions were observed, with both devices maintaining well-defined transfer curves and on/off characteristics. These results collectively demonstrate that the stretchable transistors exhibit stable electrical performance under repeated operation, electrical bias, and short-term ambient exposure.

We further investigated the materials and microstructures under mechanical stretching to understand the stable electrical performance of both stretchable transistors. For stretchable n-type transistors, two different structures were prepared: (i) PDMS/m-CNT–doped N2200 and (ii) PDMS/m-CNT–doped N2200/PU. Macroscale cracks (~tens of micrometers wide) appeared under strain in the first structure (fig. S12, A and B). For the second configuration, fig. S12 (C and D) shows an enhanced crack resistance, which can be attributed to the elastomer-semiconductor-elastomer structure (*35*, *36*). The PU encapsulation applies a counteracting shear stress from the top surface, while the PDMS substrate exerts stress from the bottom. These opposing forces synergistically suppress crack propagation by increasing the critical crack length of the N2200 film. Furthermore, the robust adhesive interfaces between N2200/PDMS and PU/N2200 effectively delocalize stress concentrations, thereby increasing the crack onset strain and preventing failure (*37*). The PU dielectric also inhibits crack formation and propagation in the second structure (fig. S12, C to E), contributing to its improved stability. For stretchable p-type transistors, the stretching mechanism was investigated by AFM. The s-CNTs formed a network structure that interacts with each other through van der Waals interactions, slide during stretching, and reorient themselves along the stretching direction (fig. S13) (*38*, *39*). Upon release, the s-CNT network returned to its original state with minimal degradation. These results demonstrate the crucial role of

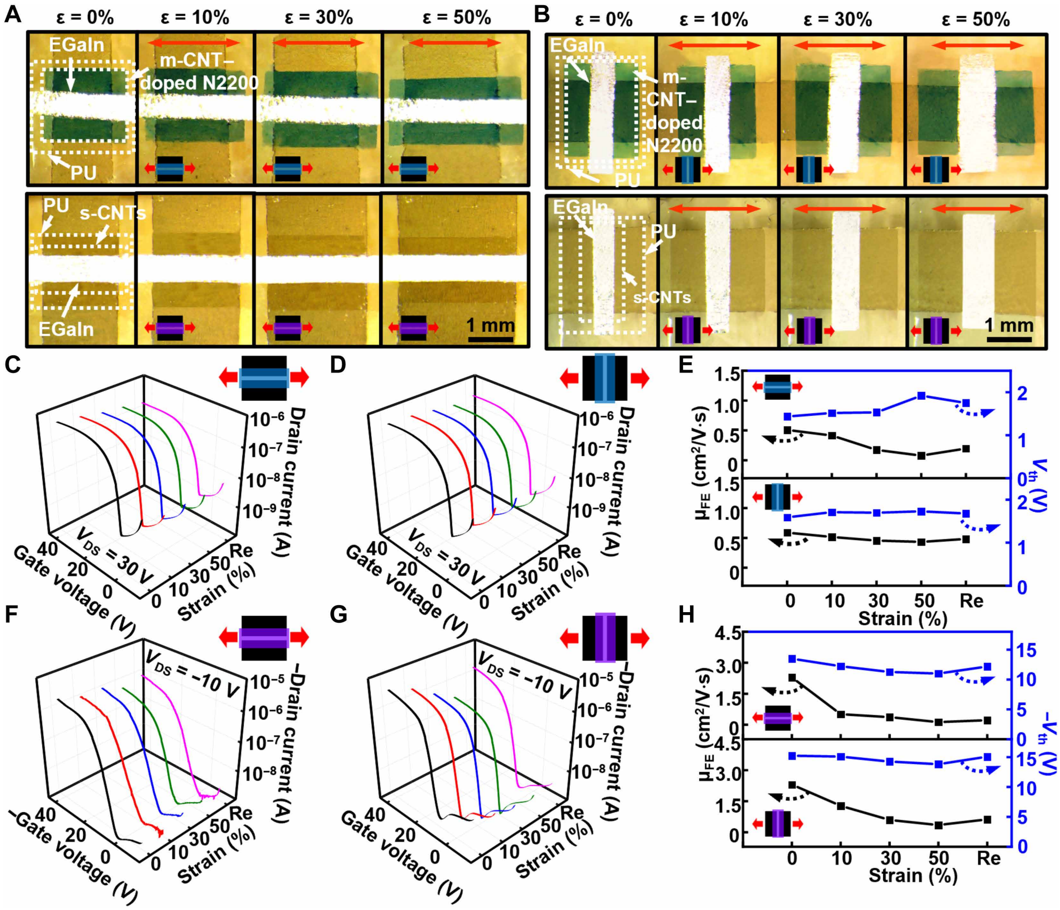

Fig. 2. Stretchable n-type and p-type transistors under mechanical strain. (**A** and **B**) Sequential optical microscopic images of the stretchable transistors under mechanical strains of 0, 10, 30, and 50% perpendicular (A) and along (B) to the channel length direction. The top row shows the stretchable n-type transistors fabricated from m-CNT–doped N2200, while the bottom row shows the stretchable p-type transistors fabricated from s-CNTs. (**C** and **D**) Transfer characteristics of the stretchable m-CNT–doped N2200 transistors under mechanical strains of 0, 10, 30, 50, and 0% (released) applied perpendicular (C) and along (D) to the channel length direction. (**E**) Calculated μ_{FE} and V_{th} of the stretchable m-CNT–doped N2200 transistor under mechanical strains of 0, 10, 30, 50, and 0% (released), shown for both perpendicular (top) and along (bottom) to the channel length direction. (**F** and **G**) Transfer characteristics of the stretchable s-CNT transistors under mechanical strains of 0, 10, 30, 50, and 0% (released) applied perpendicular (F) and along (G) to the channel length direction. (**H**) Calculated μ_{FE} and $-V_{th}$ of the stretchable s-CNT transistors under mechanical strains of 0, 10, 30, 50, and 0% (released), shown for both perpendicular (top) and along (bottom) to the channel length direction.

the elastomer-semiconductor-elastomer structure and the s-CNT network in preserving the electrical performance of the transistors under mechanical strain.

A 5 × 5 array of stretchable transistors, incorporating either m-CNT–doped N2200 transistors for n-type or s-CNT transistors for p-type, was fabricated to assess the reliability and uniformity of the devices. Figure 3A presents a schematic illustration and optical image of the stretchable transistor array, with the fabrication process detailed in Materials and Methods and illustrated in fig. S14. The array was subjected to various mechanical deformations, including stretching, bending, and poking, as shown in Fig. 3B. The μ_{FE}, V_{th}, and I_{on}/I_{off} maps of the arrays are shown in Fig. 3 (C to H), with the distributions in fig. S15. The highest μ_{FE} achieved in the stretchable n-type transistor array is 0.914 cm^2/V·s with an average of 0.449 cm^2/V·s. In contrast, the stretchable p-type transistor array achieved the highest μ_{FE} of 4.192 cm^2/V·s with an average μ_{FE} of 1.418 cm^2/V·s. The average V_{th} and I_{on}/I_{off} of stretchable n-type transistor array were 1.70 V and 0.5 × 10^3, respectively, while the stretchable p-type transistor array exhibited an average V_{th} of −10.22 V and I_{on}/I_{off} of 1.34 × 10^3. The uniform operation of all 25 devices within the array underscores the high reliability, reproducibility, and scalability of both the stretchable n-type and p-type transistors, resulting in a 100% functional device yield.

While this centimeter-scale demonstration confirms spatial uniformity, further scaling will require better control over CNT dispersion stability and surfactant chemistry to ensure reproducibility across large areas. In addition, stencil masking, while effective for prototyping, limits resolution and throughput. Scalable patterning approaches such as screen printing, ink jet printing, or photopatternable liquid metals are compatible with our soft-matter system and offer a feasible route toward manufacturing-ready stretchable electronics.

Stretchable complementary logic circuits

Building on the stable performance of the stretchable transistors, we further integrated them into complementary logic circuits,

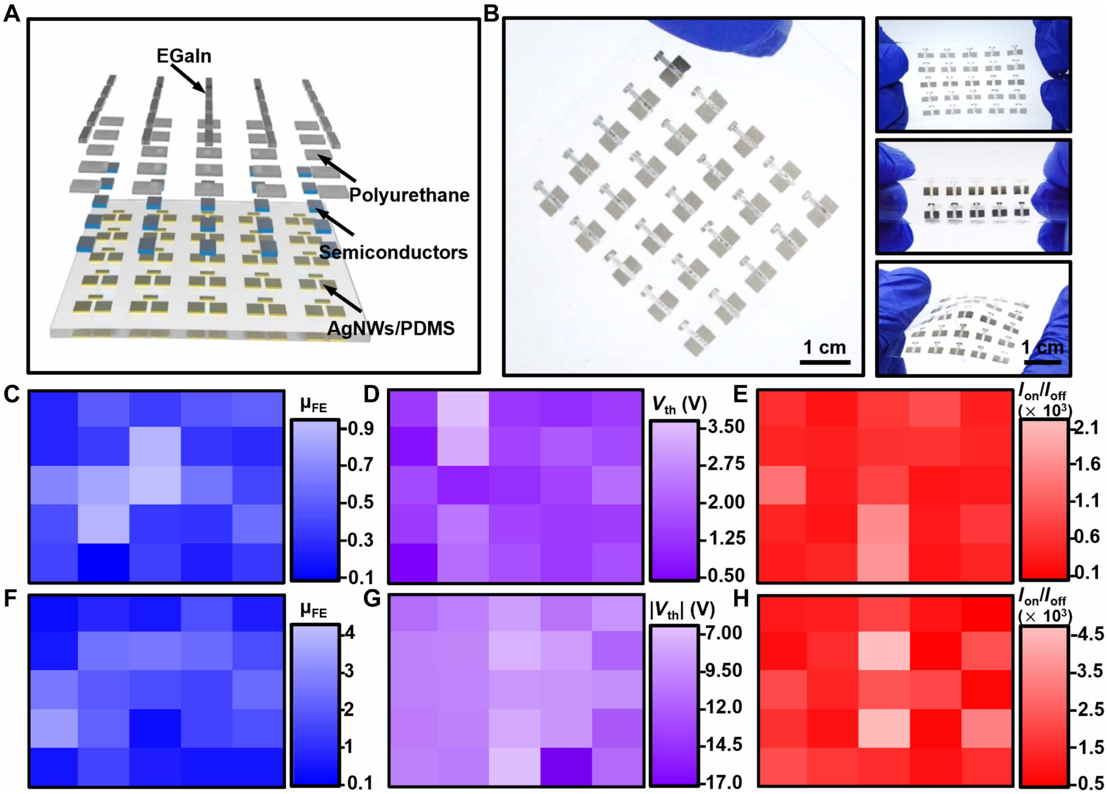

Fig. 3. Stretchable n-type and p-type transistors array. (**A**) An exploded schematic view of stretchable transistor array. (**B**) Optical image of fabricated stretchable transistor array under various mechanical deformation modes, including stretching, bending, and poking. (**C** to **E**) Calculated μ_{FE}, V_{th}, and I_{on}/I_{off} maps of 5-by-5 stretchable m-CNT–doped N2200 transistor array, respectively. (**F** to **H**) Calculated μ_{FE}, V_{th}, and I_{on}/I_{off} map of 5-by-5 s-CNT stretchable transistor array, respectively.

including inverter, NAND, and NOR gates. Figure 4A illustrates the stretchable inverter in an exploded view alongside its circuit diagram. The stretchable inverter consists of an s-CNT transistor on top and an m-CNT–doped N2200 transistor on the bottom. The channel was designed with the same length but a width ratio of 1:4 to match the on current between the two transistors. No cracks were observed before and after stretching the stretchable inverter (Fig. 4B). Figure 4 (C and D) presents the voltage transfer curve (VTC) under 0, 10, 20, 30, and 0% (released) strain applied both perpendicular and parallel to the channel length direction. The VTCs were obtained by measuring the output voltage (V_{out}) while applying a constant power supply voltage (V_{DD}) of 10 V and sweeping the input voltage (V_{in}) from 0 to 10 V, with all signals referenced to a common ground (GND). Forward and reverse voltage sweeps of the inverter revealed a hysteresis window of ~1.95 V. Nevertheless, the device maintains stable output states and a voltage gain exceeding 1, confirming reliable complementary logic behavior (fig. S16). Figure S17 shows the load curves of both transistors, indicating that most operating points are located either at the high or low output levels. This enables a sharp switch between high and low V_{out} as the V_{in} changes, resulting in a narrow transition zone. The voltage gains and switching threshold voltage (V_m) under different strains are summarized in Fig. 4E, demonstrating that the inverter maintains stable performance despite mechanical deformation. In addition, fig. S18 provides a comparison of the inverter's behavior at different V_{DD} levels, further confirming its adaptability under varying operating conditions.

The amplifying performance of the stretchable inverter was evaluated by focusing on its transition zone (Fig. 4F). Optimization of input frequency revealed a reduction in gain from 1.34 to 0.98 as the frequency increased, with the maximum gain observed at 10 mHz (fig. S19). A 10-V sinusoidal alternating current signal at 10 mHz was applied, resulting in an amplifying effect within the 3- to 18-V range. The device exhibited a decrease in gain but maintained stable operation under 30% strain when subjected to strain both perpendicular and parallel to the channel direction (Fig. 4, G and H). The reduction in performance was attributed to the high hysteresis observed in s-CNT transistors (fig. S8), primarily caused by the interface and surface traps, which critically affected the inverter's dynamic response. Further improvements could be achieved by employing other fabrication methods, using different dielectric materials, reducing dielectric thickness, and optimizing the scan rate (*40*–*43*).

To further validate the functionality of stretchable complementary logic circuits, we fabricated stretchable NAND and NOR gates, each comprising four transistors. All logic gates were therefore evaluated under quasistatic conditions consistent with the inverter's stable frequency range. The NAND gate was constructed using two parallel p-type transistors and two series n-type transistors, while the NOR gate was composed of two series p-type transistors and two parallel n-type transistors. Figure 5 (A and F) shows the schematic illustrations of stretchable NAND and NOR gates in an exploded view and their circuit diagrams. Optical images of stretchable NAND and NOR gates before (left) and after (right) mechanical

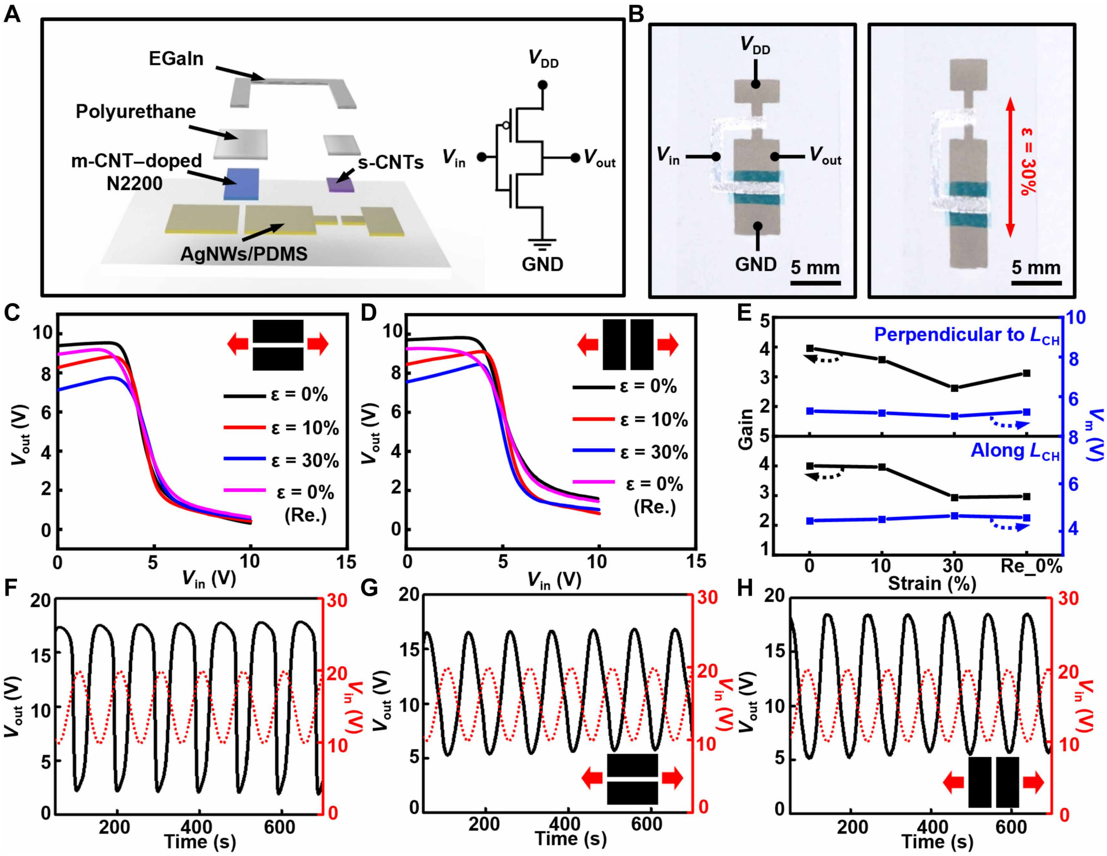

Fig. 4. Stretchable complementary inverter. (**A**) An exploded schematic view of the stretchable complementary inverter. The inset shows the circuit diagram of the complementary inverter. (**B**) Optical images of the stretchable complementary inverter before and after stretching. (**C** and **D**) VTC of the stretchable complementary inverter under mechanical strains of 0, 10, 30, and 0% (released), applied perpendicular (C) and along (D) to the channel length direction. (**E**) Voltage gain and V_m of the stretchable complementary under mechanical strains of 0, 10, 30, and 0% (released), applied perpendicular and along to the channel length direction. (**F** to **H**) Amplification performance of the stretchable complementary inverter before (F) and after stretching under the strain of 30%, shown for both perpendicular (G) and along (H) to the channel length direction.

stretching are shown in Fig. 5 (B and G). For logic function characterization, the NAND gate was tested under a constant V_{DD} of 20 V and the NOR gate under 30 V, with $V_{in,A}$ and $V_{in,B}$ switched between 0 V (logic state "0") and 30 V (logic state "1"). The truth table and static output characteristics of these stretchable logic gates are shown in fig. S20. Figure 5C shows the dynamic response of the stretchable NAND gate, which maintained logic state 0 when both inputs were at logic state 1. The device remained fully operational with no significant degradation in performance under 30% strain, as shown in Fig. 5 (D and E). Similarly, the stretchable NOR gate retained normal functionality, holding logic state 0 when both inputs were at logic state 1 (Fig. 5, H to J). These results demonstrate that stretchable complementary logic circuits, including inverters, NAND, and NOR gates, can undergo substantial mechanical deformation while preserving full electrical functionality, thereby confirming their robustness and potential for wearable devices (*6*).

The current device configuration emphasizes mechanical compliance, which introduces trade-offs in operating voltage, switching speed, and hysteresis. These limitations largely originate from the use of thick PU dielectrics and nonoptimized interface layers. Incorporating thinner or high-κ elastomeric dielectrics, ion-gel layers, or refined device geometries could significantly enhance performance while remaining compatible with the existing architecture. While the present logic circuits operate at low frequencies, this remains sufficient for tactile interactions (<1 Hz) typical of human-machine interfaces, such as touch and pressure sensing. These characteristics align with system-level requirements in applications such as prosthetic sensing and soft robotics, where reliable operation under deformation is prioritized over high-speed logic.

Stretchable tactile sensing skin

The stretchable transistors and complementary logic circuits have shown high reliability, uniformity, and stable performance, enabling their use in more complex device structures. To demonstrate this, we fabricated a stretchable tactile sensing skin, which integrates a 3 × 3 stretchable complementary inverter active matrix and s-TENG array. The integration of a complementary inverter at each pixel defines a clear logic threshold and functions as a digital gate, enabling selective activation of individual nodes while suppressing cross-talk by isolating triboelectric signals from unaddressed pixels. Figure 6A shows the schematic illustration of the stretchable tactile sensing skin, where the complementary inverter active matrix is connected to the s-TENG array using conductive rubber paste as the interconnect. The fabrication process is detailed in Materials and Methods

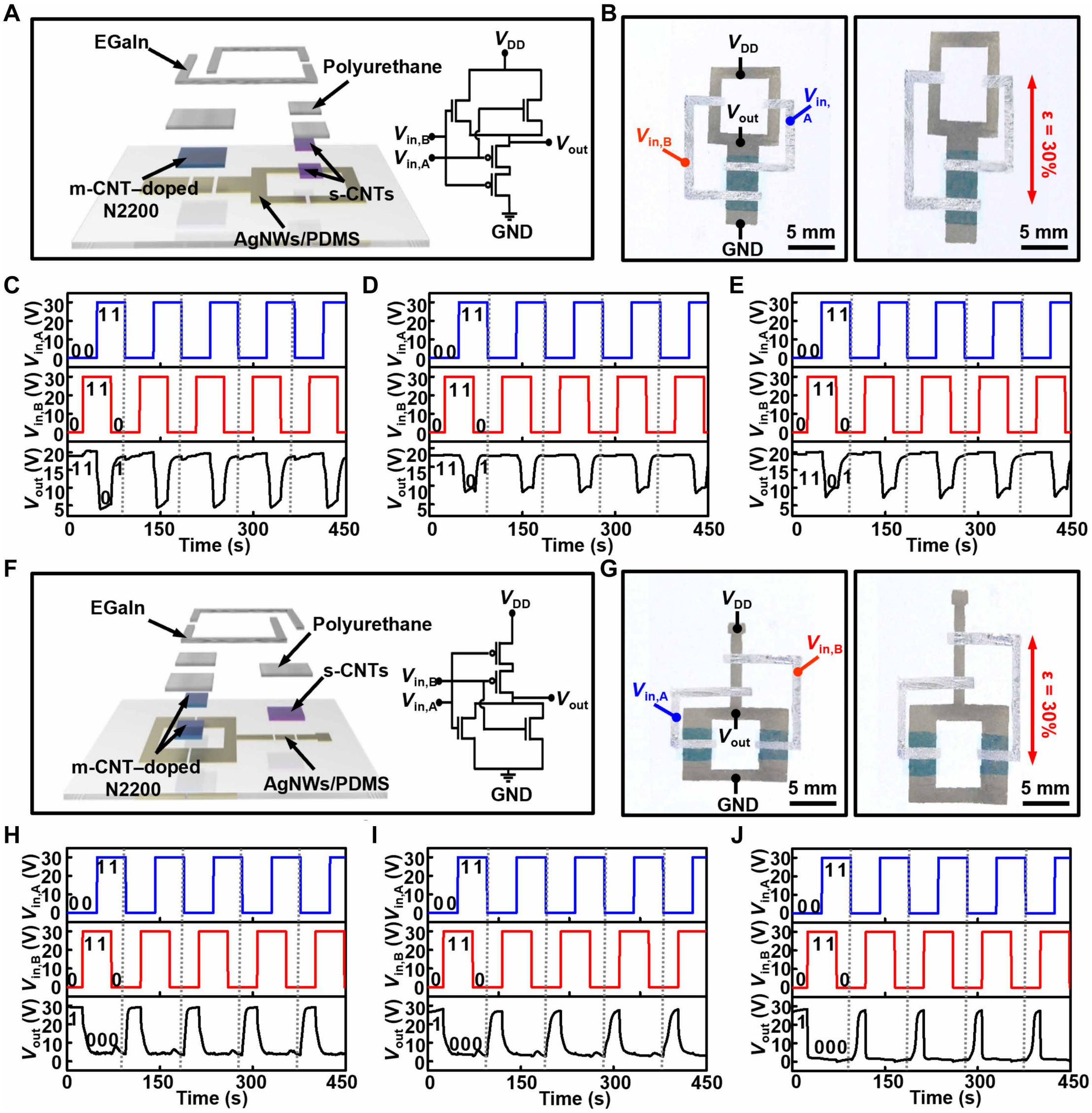

Fig. 5. Stretchable NAND and NOR gates. (**A**) An exploded schematic view of stretchable NAND gate. The inset shows the circuit diagram of the NAND gate. (**B**) Optical image of stretchable NAND gate before and after stretching. (**C** to **E**) Output characteristics of the stretchable NAND gate under V_{DD} of 30 V before (C) and after stretching under the strain of 30%, applied perpendicular (D) and along (E) to the channel length direction. (**F**) An exploded schematic view of stretchable NOR gate. The inset shows the circuit diagram of the NOR gate. (**G**) Optical image of stretchable NOR gate before and after stretching. (**H** to **J**) Output characteristics of the stretchable NOR gate under V_{DD} of 30 V before (H) and after stretching under the strain of 30%, applied perpendicular (I) and along (J) to the channel length direction.

and illustrated in fig. S21. Optical images of the stretchable tactile sensing skin before and after mechanical stretching are shown in Fig. 6B. The circuit diagram of a single tactile sensing pixel (Fig. 6C) shows each inverter connected to a word line (V_{WL}) for input and a bit line (V_{BL}) for output, with the voltage generated by the s-TENG device supplying the V_{DD} for the inverter. The full circuit diagram of the 3 × 3 tactile sensing array is shown in fig. S22.

The performance of the s-TENG device was first evaluated by measuring the voltage generated before and after mechanical stretching (fig. S23). During touch and release the touch pad, free electrons transferred between the AgNW electrode and ground, generating electric potential difference and induced current (*44*–*46*). No substantial change in the performance was observed under 30% strain in both stretching directions. Each s-TENG pixel in the array operated independently without being affected by the surrounding s-TENG pixels, demonstrating the s-TENG array's potential for its application as a part of sensory skin (fig. S24). The integration of stretchable inverters was further assessed. Figure 6D shows the output voltage of a single pixel when the tactile sensing skin was off and on controlled by stretchable inverter. The pixel was "off" when a high voltage (10 V) was applied and "on" when a low voltage (0 V) was applied. The output voltage from the bit line matched the voltage generated by the s-TENG in the on state, while no response was recorded in the off state. Figure 6 (E and H) demonstrates two different touch ways on the tactile sensing skin, while Fig. 6 (F and I) provides the corresponding voltage mapping outputs without strain. The mapping was generated by calculating the difference between the maximum voltage (V_{max}) and the

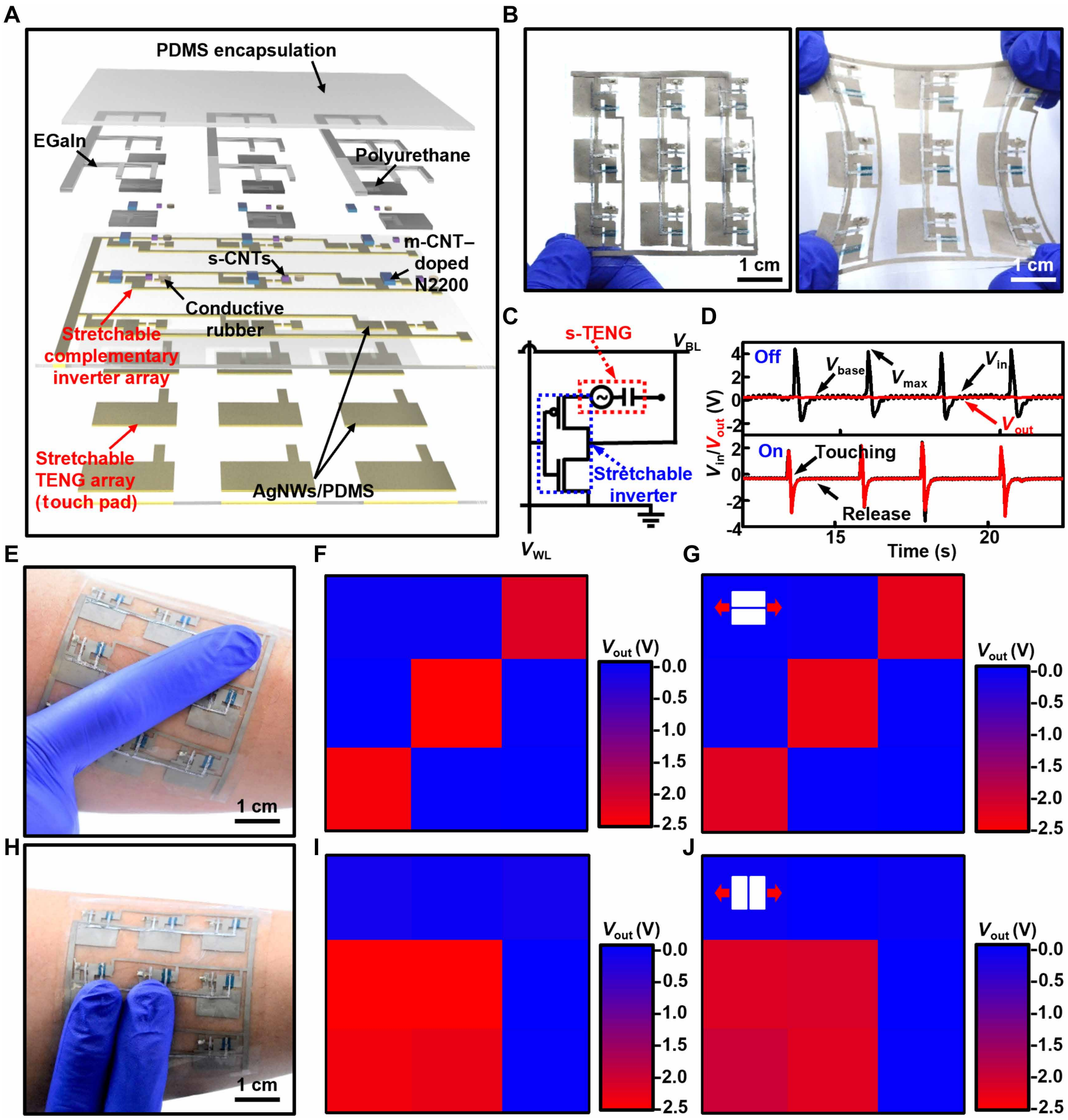

Fig. 6. Stretchable tactile sensing skin. (**A**) An exploded schematic view of the stretchable tactile sensing skin integrating a 3 × 3 stretchable complementary inverter active matrix with an s-TENG array. (**B**) Optical image of the stretchable tactile sensing skin before (left) and after stretching (right). (**C**) Circuit diagram of a single tactile sensing pixel. (**D**) Output voltage characterization of a single pixel when the device was off (top) and on (bottom). (**E** and **H**) Optical image of the stretchable tactile sensing skin with touching. (**F** and **G**) Output mapping results of the stretchable tactile sensing skin before (F) and after stretching under the strain of 30% applied perpendicular (G) to the channel length direction. (**I** and **J**) Output mapping results of the stretchable tactile sensing skin before (I) and after stretching under the strain of 30% applied along (J) to the channel length direction.

baseline voltage (V_{base}). Regions showing substantial voltage shifts were highlighted in red, indicating detected touch events. No notable change in output voltage was detected when the skin was stretched to 30% of its original length in either stretching directions (Fig. 6, G and J), confirming the stretchable tactile sensing skin's robustness under mechanical deformation.

DISCUSSION

In summary, we report a fully stretchable complementary electronics platform based on mechanically robust n-type transistors using m-CNT–doped N2200 and p-type transistors comprising s-CNT networks. The use of a stacked elastomer-semiconductor-elastomer structure for the n-type devices and a percolated nanotube network for the p-type counterparts enables stable electrical operation under mechanical strains up to 50%. These advances allow the realization of stretchable complementary logic circuits—including inverters, NAND, and NOR gates—with reliable function under 30% strain. As a demonstration of system-level integration, we developed a stretchable tactile sensing skin that combines a complementary inverter active matrix with a triboelectric nanogenerator array, highlighting the potential of this technology for self-powered, multifunctional sensing interfaces. Together, these results establish a scalable materials and device framework for intrinsically stretchable complementary electronics, offering a foundation for future classes of deformable, skin-like computing systems for use in healthcare monitoring, soft robotics, and next-generation human-machine interfaces.

MATERIALS AND METHODS

Materials

N2200 (molecular weight = 79 kDa, polydispersity index = 2.6) was obtained from Sigma-Aldrich and used without any further purifications. Tetrahydrofuran (THF; ≥99.9%), mesitylene (98%), 3-aminopropyltriethoxysilane (APTES), multiwalled CNTs (material category: 724769; outer diameter: 6 to 9 nm; length: 5 μm; purity: >95%; and conducting type: metallic), EGaIn (≥99.99%), and PU were all from Sigma-Aldrich. PDMS rubber (SYLGARD 184 silicone elastomer kit) was from Dow Corning. AgNW solution (material category: AW090; diameter range: 75 to 105 nm; length range: 15 to 45 μm; and purity: ~99.96%) was from Zhejiang Kechuang Advanced Materials Co. Ltd. Single-walled CNTs (IsoNanotubes-S; mean diameter: 1.4 nm; mean length: ~0.5 μm, purity: 98%; and conducting type: semiconducting) was from NanoIntegris Technologies Inc. and used with dilution.

Preparation of AgNW/PDMS electrodes

The AgNW/PDMS electrode was prepared by drop casting the AgNW solution (0.5 wt % in isopropanol) onto a precleaned glass slide, which was covered by the designed shadow mask fabricated by a preprogrammed cutting machine (Silhouette Cameo). After drying out under 90°C for 10 min, the shadow mask was removed, and the temperature was increased to 200°C for 30 min to enhance conductivity. Then, the PDMS precursor [10:1 (w/w) prepolymer/curing agent] was spin coated onto the previously patterned AgNW substrate at 300 rpm for 60 s and cured in an oven at 90°C for 4 hours to fully solidify. Last, the stretchable AgNW/PDMS electrode was obtained by peeling off the solidified PDMS, which embedded with AgNW from the glass slide.

Preparation of PU dielectric solution, N2200/m-CNT composite, and s-CNT solution

The PU dielectric solution was prepared by dissolving the PU into THF with the concentration of 75 mg/ml under 70°C for 2 hours. The preparation of N2200/m-CNTs composite involved preparing the N2200 solution, m-CNT suspension, and mixing the above solutions with desired ratio. The N2200 was dissolved in the mesitylene (10 mg/ml) at room temperature for 24 hours. The m-CNTs were dispersed in mesitylene with the concentration of 0.01, 0.1, 0.2, and 0.3 mg/ml by applying ultrasonication with consecutive tip sonication for 2 hours and bath sonication for 5 hours. Thereafter, N2200/m-CNT composite with different m-CNT contents (0.1, 1, 2, and 3 wt %) was obtained by mixing the N2200 solution with the preprepared m-CNT suspension (0.01, 0.1, 0.2, and 0.3 mg/ml) with the volume ratio of 1:1, respectively, followed by 5 hours of bath sonication. The s-CNT solution was prepared by diluting the bulk solution from 10 to 0.1 μg/ml with deionized water to match the current level of the n-type transistor, which was discussed above and was followed by bath sonication for 20 min.

Fabrication of stretchable n-type transistor, p-type transistor, transistor array, inverter, NAND, and NOR gates

The fabrication of the stretchable transistors involved the preparation of stretchable AgNW/PDMS source and drain electrodes, spin coating the semiconductors and PU dielectric solution. However, on the basis of different types of transistors, slight modification was applied to source and drain electrodes. APTES-modified electrode was used for p-type transistors to increase the adhesion between the s-CNTs and AgNW/PDMS source and drain electrodes. The APTES-modified electrode was prepared by exposing the stretchable AgNW/PDMS source and drain electrodes to the ultraviolet ozone for 18 min, followed by dropping 1 wt % APTES solution onto the channel region, which is prepared for p-type transistor for 10 min. After removing the APTES droplet, the electrodes were dried with N_2 gun. To pattern the semiconductor, N2200/m-CNT composite was spin coated through a designed Kapton film–based shadow mask at 1000 rpm for 60 s and then annealed at 150°C for 30 min under the N_2 atmosphere. A total of 10 μl of s-CNT solution was drop casted through a designed Kapton film–based shadow mask onto the APTES-modified electrodes, followed by heating up to 90°C to dry the s-CNT network in the air. Then, the device was rinsed with deionized water to remove the surfactant, followed by drying in vacuum oven for 1 hour. Then, the PU dielectric was spin coated using previous PU solution (75 mg/ml) at 1000 rpm for 60 s and was annealed at 100°C for 1 hour in the N_2 environment. Last, to pattern the gate electrode, the liquid metal was aligned and applied through a designed Kapton film–based shadow mask onto the channel region.

Fabrication of stretchable tactile sensing skin

The stretchable complementary inverter active matrix and s-TENG fabrication followed the same steps as described above. Via holes were created to allow the interconnection between the stretchable complementary inverter pixel and the s-TENG placed on the backside of the active matrix. The via holes were filled by conductive rubber paste, which solidified at room temperature for 12 hours. The conductive rubber paste and s-TENG adhered to each other, and no delamination was found when they were stretched by 30%. A thin layer of PDMS [10:1 (w/w) prepolymer/curing agent] was spin coated onto the active matrix as a top encapsulation layer. To emulate mechanical deformation relevant to skin-mounted applications, the device was first prestrained to 30% uniaxial elongation. The prestretched device was then laminated onto the forearm using medical-grade adhesive tape, maintaining the prestrain during measurement. This approach allowed stable signal acquisition and reflected typical strain levels encountered during human joint motion.

Electrical characterization

The capacitance of the PU was obtained using an LCR meter (U1252B, Keysight). The surface morphology of m-CNT–doped N2200 composite and s-CNTs was examined by AFM (Asylum Research MFP-3D ORIGIN+). The electrical characterization of the electronic devices was measured by a probe station (H100, Signatone) equipped with a semiconductor characterization system (4200-SCS, Keithley Instruments Inc.). The external voltage for the inverter, NAND, and NOR gate characterization was provided by a power supply (GPS-3303, GW Instek). The output mapping from the stretchable tactile sensor array was acquired using a data acquisition system and a custom LabVIEW program. The three-word lines were driven by a PXI-6723 analog output module (National Instruments) through an SCB-68–shielded I/O connector block. The three-bit lines were interfaced to a PXI-6363 multifunction I/O module (National Instruments), also via an SCB-68 connector, for voltage readout.

Supplementary Materials

This PDF file includes:
Figs. S1 to S24
Tables S1 and S2

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